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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,055	YONEDA ET AL.	
	Examiner	Art Unit	
	Hanh T. Bui	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/04/2003; 11/01/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to application filed on December 4th, 2003 in which claims 1 to 31 are presented for examination.

Status of Claims

2. Claims 1 to 31 are pending, of which claims 1 and 28 are in independent form.

Information Disclosure Statement

3. The information disclosure statements filed on December 4th, 2003 and November 1st, 2007 comply with the provisions of 37 CFR 1.97, 1.98. They have been placed in the application file and the information referred to therein has been considered as to the merits.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "*appropriately*" in claims 1, 17, 18, and 28 is a relative term which renders the claim indefinite. The term "... *appropriately changes ...in response to contention information ...*" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For compact prosecution, the Examiner interprets the term "*appropriately changes*" to mean such as "accordingly perform additional processing operations".

6. Claims 5, 6, 11, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5, 6, 11, and 12 recite the limitation "*previous*" in line 4 of each claim. There is insufficient antecedent basis for this limitation in the claim. Since these claims are depending on the base claim 1, but the base claim does not previously mention about any clock(s). For compact prosecution, the Examiner interprets the term "*plurality of [previous] clocks*" to mean "plurality of entries".

7. Claims 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 17 and 18 are depending on the base claim 1, which recites "*a software processing method*", but claims 17 and 18 are attempting to further limit the method by

adding system element "*a compiler*" described in functional terms rather than actively reciting additional method steps.

8. Claims 2-27 and 29-31 are also rejected as being dependent on the rejected base claims 1 and 28, respectively.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-16 and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hilla et al. (US Patent 7,155,722 – hereinafter, Hilla).

Regarding claim 1:

Hilla discloses a load balancing mechanism and technique that monitors a memory interface associated with a processor resource in a processor pool.

- *a monitoring step for status of use, which monitors the status of use of a resource to be used by a processor*

(FIG. 3 and the associated text, e.g., Col. 5: lines 53-55, emphasis added; "the access monitor 500 is configured to **monitor the activity** (e.g., memory access requests) ***(status)*** over the memory interface ***(resource)***").

- *an altering step for software processes, which appropriately changes a software processing method to be executed in response to contention information obtained by the monitoring step for the status of use.*

(Col. 3: lines 29-50, emphasis added; "The access monitor is arranged to compile statistics from each processor resource of the pool and provides those statistics to a central load balancing resource for use when **determining assignment of loads** (tasks) to the various processor resources. The inventive mechanism is arranged to differentiate between active and inactive tasks ***(contention information)*** assigned to each processor resource. For example, a processor may have been assigned thousands of tasks, as in the case with mobile wireless traffic patterns, but the tasks or sessions may be idle ***(contention information)***. In this case, the processor may not be processing any information and, accordingly, is available to perform additional processing operations ***(appropriately changes)***. By **monitoring** certain memory cycles according to the inventive technique, the access monitor provides **statistics** to the central load balancer indicative of the **actual measured activity of each processor resource**. The central load balancer then only needs to keep track of the total number of sessions assigned to each processor resource to guard against reaching a predefined maximum load (task) limit. Then the load balancer may assign additional

tasks ***(appropriately changes)*** based upon ***(in response)*** the measured activity ***(contention information)*** received ***(obtained by)*** from the access monitor.").

Regarding claim 2:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the altering step for software processes comprises a plurality of executing methods that allow software to execute a process, and one of the executing methods is selected when the software is executing the process in response to contention information obtained by the monitoring step for the status of use.*

(FIG. 4 and the associated text, e.g., Col. 8: lines 26-36, emphasis added; "each field 422 of the record 420 is **software configurable** (given the static nature of the record format) such that a particular field may be programmed ***(software process)*** to reflect activity ***(contention information)*** used to determine balancing of sessions across the pool of processors. The hardware assist device 500 **cooperates** with the **software executing** on the processor 302 so that it "knows" ***(selected)*** the manner in which the software **constructed** the record 420 such that it is unambiguous as to the type of information the hardware assist device (access monitor) is monitoring").

Regarding claims 3 and 4:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the resource is a storing device for a process, and the monitoring step for the status of use monitors the status of use of the storing device.*

(FIG. 3 and the associated text, e.g., Col 5: lines 28-29, emphasis added; "The memory 400 comprises **storage locations addressable by the processor** for storing software programs and data structures").

Regarding claims 5 and 6:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the monitoring step for status of use stores the preceding statuses of use of the storing device corresponding to a plurality of previous clocks so that the contention information is generated based upon the previous and current statuses of use.*

(FIG. 5 and the associated text, e.g., Col. 6: lines 52-56, and Col. 7: lines 35-59, emphasis added; "The data structure is preferably an active session table 520 having a **plurality of entries** 522, each of which is associated with a corresponding session and configured to **store status information, such as statistics, pertaining to activities associated with that session**" and "the status information stored within each entry of the active session table represents **activity (accesses)** to the session associated with that entry within a particular time interval. During a predefined interval, each access by a processor 302 to a particular session block 420 is **recorded** within the active session table 520 as an increment ***(preceding statuses/previous clocks)*** to the status information stored within the associated entry 522. The active session table 520 thus keeps track of which sessions had a "hit" during the interval of time, thereby indicating an active session... the central load balancer interface logic 516 provides to the central

load balancer 250 a count as to the number of active sessions ***(in use)*** its associated processor 302 processed during the **previous time** interval").

Regarding claims 7 and 8:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the monitoring step for status of use stores the time of use when the storing device is in use, and based upon whether or not the time of use is not less than a predetermined value, the contention information is generated.*

(FIG. 5 and the associated text, e.g., Col. 7: lines 16-34, emphasis added; "Over a period of time, certain active entries 522 may be **"aged out"** of the table 510 to allow insertion of more recent active sessions within those entries. The active session table 520 **keeps track of the activity of sessions** within the session region 410 of memory 400 during that time period. Upon being presented a decoded address over line 510 from the address decode logic 508, the session update logic 512 (i) updates the appropriate entry 522 (if it exists) by, e.g., incrementing status information contained within the entry or (ii) creates a new entry of the table 520. Specifically, the session update logic 512 **compares** that address ***(predetermined value)*** with the address of a session stored within each entry 522 of the active session table 520. If there is not a match, the session update logic 512 allocates an entry by executing an aging algorithm to remove an existing entry from the table 520 and insert the current session identified by the decoded address into that entry. The aging algorithm may be based on, e.g., a

count of the number of accesses made by a processor 302 to the session block/record 420 associated with the entry").

Regarding claims 9 and 10:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the resource comprises a storing device for a process and a bus that connects the processor to the storing device, and the monitoring step for status of use monitors the status of use of the bus.*

(FIG. 3 and the associated text, e.g., Col. 5: lines 25-29 and lines 39-40, emphasis added; "Each resource 300 preferably comprises a processor 302 coupled to a memory 400 via a **memory bus or interface 310**. The memory 400 comprises **storage locations** addressable by the processor for storing software programs and data structures" and "The memory interface 310 ***(bus)*** comprises a plurality of wires or "lines," including memory address, data and control lines ... **monitors** the physical signals on the interface 310 ***(bus)*** to determine the active/inactive status of sessions distributed among the processor resources").

Regarding claims 11 and 12:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the monitoring step for status of use stores the preceding statuses of use of the bus corresponding to a plurality of previous clocks so that the contention information is generated based upon the previous and current statuses of use.*

(FIG. 5 and the associated text, e.g., Col. 6: lines 34-37, emphasis added; "The access **monitor** comprises memory interface logic 502 coupled to the memory interface 310 and to address decode logic 508. The memory interface logic 502 provides a physical interface to the **memory interface "bus" including buffers and transceivers that receive and output information over the bus**").

Regarding claims 13 and 14:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the monitoring step for status of use stores the time of use when the bus is in use, and based upon whether or not the time of use is not less than a predetermined value, the contention information is generated.*

(FIG. 5 and the associated text, e.g., Col. 7: lines 16-34, emphasis added; "Over a period of time, certain active entries 522 may be **"aged out"** of the table 510 to allow insertion of more recent active sessions within those entries. The active session table 520 **keeps track of the activity of sessions** within the session region 410 of memory 400 during that time period. Upon being presented a decoded address over line 510 from the address decode logic 508, the session update logic 512 (i) updates the appropriate entry 522 (if it exists) by, e.g., incrementing status information contained within the entry or (ii) creates a new entry of the table 520. Specifically, the session

update logic 512 **compares** that address ***(predetermined value)*** with the address of a session stored within each entry 522 of the active session table 520. If there is not a match, the session update logic 512 allocates an entry by executing an aging algorithm to remove an existing entry from the table 520 and insert the current session identified by the decoded address into that entry. The aging algorithm may be based on, e.g., a count of the number of accesses made by a processor 302 to the session block/record 420 associated with the entry").

Regarding claim 15:

Hilla discloses *the software processing method according to claim1, wherein:*

- *the resource is a second processor that executes a process in response to a processing request from the processor, and the monitoring step for status of use monitors the status of use of the second processor.*

(FIG. 2 and the associated text, e.g., Col. 4: lines 58-60, emphasis added; "The intermediate network node 200 comprises a **multiprocessor** environment of processor resources (PS) 300 organized as a "processor pool 210"".

Examiner notes that the processor pool 210 comprises a plurality of processor resource 300, therefore the resource can be another/second processor that executes a process in response to a processing request from the processor.

FIG. 3 and the associated text, e.g., Col 5: lines 24-29, emphasis added; "FIG. 3 is a schematic block diagram of a processor resource 300 ***(second processor)*** within the processor pool 210. Each resource 300 ***(second processor)*** preferably comprises

a processor 302 coupled to a memory 400 via a memory bus or interface 310. The memory 400 comprises storage locations addressable by the processor for storing software programs and data structures".

Col. 3: lines 29-33, emphasis added; "The access **monitor** is arranged to compile statistics ***(status)*** from each processor resource of the pool").

Regarding claim 16:

Hilla discloses *the software processing method according to claim1, further comprising:*

- *a plurality of memory banks that are accessed by using the same address, wherein contention information that is obtained from the monitoring step for status of use is a signal that indicates selection of one of the memory banks.*

(FIG. 4 and the associated text, e.g., Col. 6: lines 3-18,emphasis added; "FIG. 4 is a diagram showing the address space organization of the memory 400 associated with each processor 302 of a processor resource 300. The **address space** of the memory is **apportioned** into various regions, one of which is a region 410 configured to store sessions. This "session" region 410 is further divided into various blocks 420 ***(memory banks)***, each of which is configured to store a session... the access monitor 500 **monitors** memory control lines and predetermined high-order memory address lines that map ***(selection)*** to the session region 410 and, in particular, to a specific block 420 within the session region to determine the **activity** associated with that session").

Regarding claim 28:

Hilla discloses a load balancing mechanism and technique that monitors a memory interface associated with a processor resource in a processor pool.

- *a processor; a resource that the processor uses; a monitoring device for status of use which monitors status of use of the resource; an altering device for a software process which appropriately alters a processing method of software to be executed in response to contention information obtained by the monitoring device for the status of use.*

(FIG. 2; 3 and the associated text, e.g., Col. 5: lines 24-27, emphasis added; "FIG. 3 is a schematic block diagram of a **processor resource** 300 within the processor pool 210. Each resource 300 preferably comprises a **processor** 302 coupled to a **memory** 400 via a memory bus or interface 310. The memory 400 comprises storage locations **addressable by the processor** for storing software programs and data structures"

All other limitations of this claim have been noted in the rejection of claim 1).

Regarding claim 29:

The rejection of base claim 28 is incorporated. All the limitations of this claim have been noted in the rejection of claim 2.

Regarding claim 30:

The rejection of base claim 28 is incorporated. All the limitations of this claim have been noted in the rejection of claim 15.

Regarding claim 31:

Hilla discloses *the software processing method according to claim28, wherein:*

- *the contention information is an interrupt signal to the processor.*

(Col. 5: lines 40-43, emphasis added; "the present invention provides a technique that efficiently monitors the **physical signals** on the interface 310 to determine the active/inactive status of sessions distributed among the processor resources"

Examiner notes that the physical signal as mentioned above can be an interrupt signal if the status is inactive).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 17-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hilla et al. (US Patent 7,155,722 - hereinafter, Hilla) in view of Trissel et al. (US Patent 5,274,815 - hereinafter, Trissel).

Regarding claims 17 and 18:

Hilla discloses *the software processing method according to claim 1*, further comprising:

- *a compiler, wherein the compiler adds to software the following means and processes: a process identifying means which identifies whether or not a process uses the resource from software; an equivalent process that is equivalent to the process identified by the process identifying means, and does not use the resource ; a determining process for the status of use, which determines the status of use based upon contention information obtained in the step of monitoring the status of use ; and a substituting process which substitutes the equivalent process appropriately for the process identified by the process-identifying means based upon the results of the determining process for the status of use.*

(Col. 6: lines 43-45, Col. 8: lines 26-36, emphasis added; "the control lines 504 may specify either a **read or write operation** to a specific session block/record 420 identified by the address lines 506" and "each field 422 of the record 420 is software **configurable** (given the static nature of the record format) such that a particular field may be **programmed** to reflect activity used to determine balancing of sessions across the pool of processors. The hardware assist device 500 **cooperates with the software executing on the processor** 302 so that it "knows" the manner in which the software constructed the record 420 such that it is unambiguous as to the type of information the hardware assist device (access monitor) is monitoring."

Examiner notes that any piece of executable software is made up of means and processes, which is almost always in order to implement changes to software, it always does it through the use of a compiler, but Hilla does not explicitly disclose with a compiler.)

However, Trissel further discloses a dynamic instruction modifying controller and operation method, wherein the background teaches more clearly about the use of compiler "The most primitive way to **alter a computer program is to edit the computer program**, make all modifications desired by **changing instructions in the computer program,** compile, link, and execute the code to observe changes... **Compiler options are statements or commands which alter the course of the compilation process** such as to determine optimization levels and enable debugging modes or facilities, and/or gather statistical information. By changing, deleting, or **adding** compiler options, a user or a programmer can **alter the performance**, execution flow, or results of a computer program. Compiler options are widely used because they are, in most cases, easier to implement than other technologies" (See Col. 1: lines 25-40).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the teachings of Trissel into the teachings of Hilla because such combination would have achieved flexibility and control of software as suggested by Trissel (See Col. 1: lines15-16).

Regarding claims 19 and 20:

Hilla discloses *the software processing method according to claim 1 wherein:*

- *the contention information is processing time from the issuance of the processing request for the resource until the completion of the process, and the determining process for the status of use is a process which compares the processing time to a preset value.*

(Col. 7: line 60 through Col 8: line 15, emphasis added; "the central load balancer 250 analyzes the status information provided by each access monitor 500 of a processor resource 300 to determine the actual load ***(processing time)*** executed by the resource during a specified period of time...It will be understood to those skilled in the art that various forms of status information may advantageously be gathered in accordance with the principles of the present invention. The types of statistics ***(determining process)*** that may be collected include the number of active sessions during a predetermined time interval ***(preset value)***, the number of "hits" (accesses) to a particular session block during a time interval and the number of creations/destroys of sessions during that interval.").

Regarding claims 21 and 22:

Hilla discloses *the software processing method according to claim 1 wherein:*

- *the contention information is waiting time from the issuance of the processing request for the resource until the start of the process, and the determining process for the status of use is a process which compares the waiting time to a preset value.*

(Col 8: lines 3-15, emphasis added; "It will be understood to those skilled in the art that various forms of status information ***(contention information)*** may advantageously be gathered in accordance with the principles of the present invention. The types of statistics ***(determining process)*** that may be collected include the number of active sessions during a predetermined time interval ***(preset value)***, the number of "hits" (accesses) to a particular session block during a time interval and the number of creations/destroys of sessions during that interval ***(waiting time)***").

Regarding claims 23 and 24:

Hilla discloses *the software processing method according to claim 1 wherein:*

- *the determining process for status of use reexamines the determination for the status of use of the resource regularly or irregularly.*

(Col. 7: lines 64-67, emphasis added; "the central load balancer may overlay the number of active sessions per processor onto the total number of sessions assigned per processor to determine the type of activity ***(regular)*** versus inactivity ***(irregularly)*** (quiescence) across the pool of resources")

Regarding claims 25 and 26:

Hilla discloses *the software processing method according to claim 1 wherein:*

- *the determining process for status of use reexamines the determination for the status of use of the resource by using random numbers.*

(FIG. 5 and the associated text, e.g., Col. 6: lines 37-45, emphasis added; "The logic 502 also provides address lines 504 and control lines 506 ***(random numbers)*** to the address decode logic 508. The address decode logic 508 is configured with conventional circuitry adapted to decode the information presented over the lines 504, 506 in order to **determine** the operations performed by the processor 302 for a specific session").

Regarding claim 27:

Hilla discloses *the software processing method according to claim 1 wherein:*

- *in the case when processes to be extracted by the process-identifying means are extracted from a plurality of portions of the software, the compiler further adds to the software an identifying process for identifying the portions of appearance of the processes identified by the process-identifying means, and the storing process stores the contention information for each of the portions of appearance so that the determining process for status of use carries out the determination by using the contention information stored for each of the portions of appearance.*

(Col. 8: lines 26-36, emphasis added; "each field 422 of the record 420 is software **configurable** (given the static nature of the record format) such that a particular field may be **programmed** to reflect activity used to determine balancing of sessions across the pool of processors. The hardware assist device 500 **cooperates with the software executing on the processor** 302...")

Trissel further discloses a dynamic instruction modifying controller and operation method, wherein the background teaches more clearly about the use of compiler "The most primitive way to **alter a computer program is to edit the computer program**, make all modifications desired by **changing instructions in the computer program,** compile, link, and execute the code to observe changes... **Compiler options are statements or commands which alter the course of the compilation process** such as to determine optimization levels and enable debugging modes or facilities, and/or gather statistical information. By changing, deleting, or **adding** compiler options, a user or a programmer can **alter the performance**, execution flow, or results of a computer program. Compiler options are widely used because they are, in most cases, easier to implement than other technologies" (See Col. 1: lines 25-40).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh T. Bui whose telephone number is (571) 270-1976. The examiner can normally be reached on Mon. - Thur., 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

_BH_

TUAN DAM
SUPERVISORY PATENT EXAMINER